Abstracts

A 2 Gb/s Throughput GaAs Digital Time Switch LSI Using LSCFL (1985 [MCS])

T. Takada, Y. Shimazu, K. Yamasaki, M. Togashi, K. Hoshikawa and M. Idda. "A 2 Gb/s Throughput GaAs Digital Time Switch LSI Using LSCFL (1985 [MCS])." 1985 Microwave and Millimeter-Wave Monolithic Circuits Symposium Digest 85.1 (1985 [MCS]): 22-26.

A GaAs four channel digital time switch having a 2.0 Gb/s throughput is developed. Low Power Source Coupled FET Logic (LSCFL) and 0.55 µm gate length buried p-layer SAINT-FETs are applied. The switch includes 1176 devices (FETs, diodes, and resistors). The 75 % fabrication yield is attained using dislocation free wafers.

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